AMENDMENTS TO THE CLAIMS:

1. (Currently amended) An image display device, comprising:

a pixel array portion including k (k is an integer not less than 2) signal lines, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the k signal lines; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes shift registers to which m-bit (m is a natural number) digital picture signals are inputted, the number of the shift registers being ~~m or~~ a multiple of m, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines,

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

2. (Original) A device according to claim 1, wherein the number of the D/A converter circuits is k/n.

3. (Currently amended) A device according to claim 1, wherein each of the plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

4. (Original) A device according to claim 1, wherein the storage circuit is a latch circuit.

5. (Original) A device according to claim 4, wherein the latch circuit includes an analog switch and a holding capacitance.

6. (Original) A device according to claim 4, wherein the latch circuit includes a clocked inverter.

7. (Original) A device according to claim 4, wherein the latch circuit includes an analog switch and a plurality of inverters.

8. (Original) A device according to claim 1, wherein a display is carried out using a liquid crystal material.

9. (Original) A device according to claim 1, wherein a display is carried out using an electroluminescence (EL) material.

10. (Original) A portable telephone, which uses the image display device according to claim 1.

11. (Original) A video camera, which uses the image display device according to claim 1.

12. (Original) A personal computer, which uses the image display device according to claim 1.

13. (Original) A head mount display, which uses the image display device according to claim 1.

14. (Original) A television, which uses the image display device according to claim 1.

15. (Original) A portable book, which uses the image display device according to claim 1.

16. (Original) A CVD player, which uses the image display device according to claim 1.

17. (Original) A digital camera, which uses the image display device according to

claim 1.

18. (Original) A projector, which uses the image display device according to claim 1.

19. (Currently amended) An image display device, comprising:

a pixel array portion including a plurality of signal lines, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the plurality of signal lines; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes ~~a plurality of~~ a multiple of m shift registers to which ~~multi-bit~~ m-bit (m is a natural number) digital picture signals are inputted, a plurality of storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines, and

wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

20. (Currently amended) A device according to claim 19, wherein each of the plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

21. (Original) A device according to claim 19, wherein the storage circuit is a latch circuit.

22. (Original) A device according to claim 21, wherein the latch circuit includes an analog switch and a holding capacitance.

23. (Original) A device according to claim 21, wherein the latch circuit includes a clocked inverter.

24. (Original) A device according to claim 21, wherein the latch circuit includes an analog switch and a plurality of inverters.

25. (Original) A device according to claim 19, wherein a display is carried out using a liquid crystal material.

26. (Original) A device according to claim 19, wherein a display is carried out using an electroluminescence (EL) material.

27. (Original) A portable telephone, which uses the image display device according to claim 19.

28. (Original) A video camera, which uses the image display device according to claim 19.

29. (Original) A personal computer, which uses the image display device according to claim 19.

30. (Original) A head mount display, which uses the image display device according to claim 19.

31. (Original) A television, which uses the image display device according to claim 19.

32. (Original) A portable book, which uses the image display device according to

claim 19.

33. (Original) A CVD player, which uses the image display device according to claim 19.

34. (Original) A digital camera, which uses the image display device according to claim 19.

35. (Original) A projector, which uses the image display device according to claim 19.

36. (Currently amended) An image display device, comprising:

a pixel array portion including k (k is a multiple of 3) signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the k signal lines; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB, the number of the shift registers being ~~m or~~ a multiple of m, m x k/n (n is a multiple of 3) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

37. (Original) A device according to claim 36, wherein the number of the D/A converter circuits is k/n.

38. (Currently amended) A device according to claim 36, wherein each of the

plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

39. (Original) A device according to claim 36, wherein the storage circuit is a latch circuit.

40. (Original) A device according to claim 39, wherein the latch circuit includes an analog switch and a holding capacitance.

41. (Original) A device according to claim 39, wherein the latch circuit includes a clocked inverter.

42. (Original) A device according to claim 39, wherein the latch circuit includes an analog switch and a plurality of inverters.

43. (Original) A device according to claim 36, wherein a display is carried out using a liquid crystal material.

44. (Original) A device according to claim 36, wherein a display is carried out using an electroluminescence (EL) material.

45. (Original) A portable telephone, which uses the image display device according to claim 36.

46. (Original) A video camera, which uses the image display device according to claim 36.

47. (Original) A personal computer, which uses the image display device according to claim 36.

48. (Original) A head mount display, which uses the image display device according

to claim 36.

49. (Original) A television, which uses the image display device according to claim 36.

50. (Original) A portable book, which uses the image display device according to claim 36.

51. (Original) A CVD player, which uses the image display device according to claim 36.

52. (Original) A digital camera, which uses the image display device according to claim 36.

53. (Original) A projector, which uses the image display device according to claim 36.

54. (Currently amended) An image display device, comprising:

a pixel array portion including signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, the number of the signal lines being a multiple of 3, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the signal lines, the number of which is the multiple of 3; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes ~~a plurality of~~ a multiple of m shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB, a plurality of storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and a plurality of signal line selecting circuits for transmitting

output signals of the D/A converter circuits to the corresponding signal lines,

one horizontal scan period includes a first, a second, and a third periods,

the digital picture signals corresponding to the R are inputted to the respective shift registers in the first period,

the digital picture signals corresponding to the G are inputted to the respective shift registers in the second period,

the digital picture signals corresponding to the B are inputted to the respective shift registers in the third period, and

in each of the three periods, an operation in which the inputted digital picture signals are sequentially shifted in the respective shift registers until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal, is repeated once or plural times;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

55. (Currently amended) A device according to claim 54, wherein each of the plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

56. (Original) A device according to claim 54, wherein the storage circuit is a latch circuit.

57. (Original) A device according to claim 56, wherein the latch circuit includes an analog switch and a holding capacitance.

58. (Original) A device according to claim 56, wherein the latch circuit includes a clocked inverter.

59. (Original) A device according to claim 56, wherein the latch circuit includes an analog switch and a plurality of inverters.

60. (Original) A device according to claim 54, wherein a display is carried out using a

liquid crystal material.

61. (Original) A device according to claim 54, wherein a display is carried out using an electroluminescence (EL) material.

62. (Original) A portable telephone, which uses the image display device according to claim 54.

63. (Original) A video camera, which uses the image display device according to claim 54.

64. (Original) A personal computer, which uses the image display device according to claim 54.

65. (Original) A head mount display, which uses the image display device according to claim 54.

66. (Original) A television, which uses the image display device according to claim 54.

67. (Original) A portable book, which uses the image display device according to claim 54.

68. (Original) A CVD player, which uses the image display device according to claim 54.

69. (Original) A digital camera, which uses the image display device according to claim 54.

70. (Original) A projector, which uses the image display device according to claim 54.

71. (Currently amended) A signal line driver circuit of an image display device for driving k (k is an integer not less than 2) signal lines, the signal line driver circuit comprising:

shift registers to which m-bit (m is a natural number) digital picture signals are inputted, the number of the shift registers being ~~m or~~ a multiple of m;

m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines,

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

72. (Original) A circuit according to claim 71, wherein the number of the D/A converter circuits is k/n.

73. (Currently amended) A circuit according to claim 71, wherein each of the plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

74. (Original) A circuit according to claim 71, wherein the storage circuit is a latch circuit.

75. (Original) A circuit according to claim 74, wherein the latch circuit includes an analog switch and a holding capacitance.

76. (Original) A circuit according to claim 74, wherein the latch circuit includes a clocked inverter.

77. (Original) A circuit according to claim 74, wherein the latch circuit includes an analog switch and a plurality of inverters.

78. (Original) A circuit according to claim 71, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

79. (Original) A circuit according to claim 71, wherein the driver circuit of the image display device is formed of a single crystal transistor.

80. (Currently amended) A signal line driver circuit of an image display device for driving a plurality of signal lines, the signal line driver circuit comprising:

~~a plurality of~~ a multiple of m shift registers to which ~~multi-bit~~ m-bit (m is a natural number) digital picture signals are inputted;

a plurality of storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines,

wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

81. (Currently amended) A circuit according to claim 80, wherein each of the plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

82. (Original) A circuit according to claim 80, wherein the storage circuit is a latch circuit.

83. (Original) A circuit according to claim 82, wherein the latch circuit includes an analog switch and a holding capacitance.

84. (Original) A circuit according to claim 82, wherein the latch circuit includes a clocked inverter.

85. (Original) A circuit according to claim 82, wherein the latch circuit includes an analog switch and a plurality of inverters.

86. (Original) A circuit according to claim 80, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

87. (Original) A circuit according to claim 80, wherein the driver circuit of the image display device is formed of a single crystal transistor

88. (Currently amended) A signal line driver circuit of an image display device for driving signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, the number of the signal lines being a multiple of 3, the signal line driver circuit comprising:

shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB, the number of the shift registers being ~~m or~~ a multiple of m;

m x k/n (n is a multiple of 3) storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

89. (Original) A circuit according to claim 88, wherein the number of the D/A converter circuits is k/n.

90. (Currently amended) A circuit according to claim 88, wherein each of the plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

91. (Original) A circuit according to claim 88, wherein the storage circuit is a latch circuit.

92. (Original) A circuit according to claim 91, wherein the latch circuit includes an analog switch and a holding capacitance.

93. (Original) A circuit according to claim 91, wherein the latch circuit includes a clocked inverter.

94. (Original) A circuit according to claim 91, wherein the latch circuit includes an analog switch and a plurality of inverters.

95. (Original) A circuit according to claim 88, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

96. (Original) A circuit according to claim 88, wherein the driver circuit of the image display device is formed of a single crystal transistor.

97. (Currently amended) A signal line driver circuit of an image display device for driving signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, the number of the signal lines being a multiple of 3, the signal line driver circuit comprising:

~~a plurality of~~ a multiple of m shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB;

a plurality of storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines, wherein

one horizontal scan period includes a first, a second, and a third periods,

the digital picture signals corresponding to the R are inputted to the respective shift registers in the first period,

the digital picture signals corresponding to the G are inputted to the respective shift registers in the second period,

the digital picture signals corresponding to the B are inputted to the respective shift registers in the third period, and

in each of the three periods, an operation in which the inputted digital picture signals are sequentially shifted in the respective shift registers until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal, is repeated once or plural times;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

98. (Currently amended) A circuit according to claim 97, wherein each of the plurality of ramp type D/A converter ~~circuit~~ circuits comprises a bit comparison pulse width converter circuit and an analog switch.

99. (Original) A circuit according to claim 97, wherein the storage circuit is a latch circuit.

100. (Original) A circuit according to claim 99, wherein the latch circuit includes an analog switch and a holding capacitance.

101. (Original) A circuit according to claim 99, wherein the latch circuit includes a clocked inverter.

102. (Original) A circuit according to claim 99, wherein the latch circuit includes an analog switch and a plurality of inverters.

103. (Original) A circuit according to claim 97, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

104. (Original) A circuit according to claim 97, wherein the driver circuit of the image display device is formed of a single crystal transistor.